10/707,964

1. (Currently Amended) A fin-type field effect transistor (FinFET) comprising:

a first fin structure positioned on a substrate;

a second fin structure positioned on said substrate;

first spacers adjacent said first fin structure; and

second spacers adjacent said second fin structure,

wherein said first spacers cover a larger portion of said first fin structure when compared to the portion of said second fin structure covered by said second spacers, and

wherein first spacers are larger than said second spacers and the difference in size between said first spacers and said second spacers is adapted to provide a difference between said first fin structure and said second fin structure.

2. (Currently Amended) The FinFET in claim 1, wherein ~~first spacers are larger than said second spacers and~~ the difference in size between said first spacers and said second spacers is adapted to provide a difference in doping between said first fin structure and said second fin structure.

3. (Original) The FinFET in claim 2, wherein said difference in doping between said first fin structure and said second fin structure changes an effective channel width of said first fin structure when compared to said second fin structure.

4. (Original) The FinFET in claim 1, wherein said first spacers and said second spacers include doping impurities adapted to diffuse into adjacent portions of said first fin structure and said second fin structure so as to cause the portion of each fin structure that is adjacent each spacer to comprise an electrically inactive portion of the device.

5. (Currently Amended) ~~The FinFET in claim 1,~~ A fin-type field effect transistor (FinFET) comprising:

a first fin structure positioned on a substrate;

a second fin structure positioned on said substrate;

first spacers adjacent said first fin structure; and

second spacers adjacent said second fin structure,

wherein said first spacers cover a larger portion of said first fin structure when compared to the portion of said second fin structure covered by said second spacers, and

wherein said first fin structure is the same physical size as said second fin structure.

6. (Currently Amended) ~~The FinFET in claim 1,~~ A fin-type field effect transistor (FinFET) comprising:

a first fin structure positioned on a substrate;

a second fin structure positioned on said substrate;

first spacers adjacent said first fin structure; and

second spacers adjacent said second fin structure,

wherein said first spacers cover a larger portion of said first fin structure when compared to the portion of said second fin structure covered by said second spacers, further comprising:

at least one gate conductor over said first fin structure and said second fin structure; and

a gate insulator positioned between said gate conductor and said first fin structure and said second fin structure.

7. (Original) The FinFET in claim 1, wherein said first spacers and said second spacers comprise the same material.

8. (Original) A fin-type field effect transistor (FinFET) comprising:

a buried oxide layer over a substrate;

a first fin structure positioned on said buried oxide layer;

a second fin structure positioned on said buried oxide layer;

spacers adjacent only said first fin structure;

a gate insulator covering a full length of said second fin structure.

9. (Original) The FinFET in claim 8, wherein said spacers are adapted to provide a difference in doping between the first fin structure and the second fin structure.

10. (Original) The FinFET in claim 9, wherein said difference in doping between said first fin structure and said second fin structure changes an effective channel width of said first fin structure when compared to said second fin structure.

11. (Original) The FinFET in claim 8, wherein said spacers include doping impurities adapted to diffuse into adjacent portions of said first fin structure so as to cause the portion of said first fin structure that is adjacent said first spacers to comprise an electrically inactive portion of the device.

12. (Original) The FinFET in claim 8, wherein said first fin structure is the same physical size as said second fin structure.

13. (Original) The FinFET in claim 8, further comprising at least one gate conductor over said first fin structure and said second fin structure.

14. (Original) The FinFET in claim 8, wherein said gate insulator is further positioned along portions of said first fin structure not covered by said spacers.

14. (Original) The FinFET in claim 8, wherein said first spacers and said second spacers comprise the same material.

15. (Original) A method of making a fin-type field effect transistor (FinFET) structure, said method comprising:

forming a first fin structure and a second fin structure on a substrate;

forming first spacers adjacent said first fin structure and second spacers adjacent said second fin structure; and

removing a portion of said second spacers such that said first spacers cover a larger portion of said first fin structure when compared to the portion of said second fin structure covered by said second spacers.

16. (Original) The method in claim 15, further comprising, after removing said portion of said second spacers, forming at least one gate conductor over said first fin structure and said second fin structure.

17. (Original) The method in claim 15, further comprising, before forming said gate conductor, forming a gate insulator on said first fin structure and said second fin structure.

18. (Original) The method in claim 17, further comprising, after removing said portion of said second spacers, doping portions of said first fin structure and said second fin structure that are not protected by said first spacers and said second spacers, such that there is a difference in doping between said first fin structure and said second fin structure.

19. (Original) The method in claim 18, wherein a difference in doping between said first fin structure and said second fin structure changes an effective width of said second fin structure when compared to said first fin structure.

20. (Original) The method in claim 15, wherein said first fin structure is the same size as said second fin structure, wherein said width is a measure of distance in a direction perpendicular to the surface of said buried oxide layer.

21. (Original) The method in claim 15, wherein said first spacers and said second spacers

comprise the same material.

22. (Original) A method of making a fin-type field effect transistor (FinFET) structure, said method comprising:

forming a buried oxide layer on a substrate;

forming a first fin structure and a second fin structure on said buried oxide layer;

forming first spacers adjacent only said first fin structure and second spacers adjacent said second fin structure; and

removing a portion of said second spacers.

23. (Original) The method in claim 22, further comprising, after removing said portion of said second spacers, forming at least one gate conductor over said first fin structure and said second fin structure.

24. (Original) The method in claim 22, further comprising, before forming said gate conductor, forming a gate insulator on said first fin structure, said second fin structure, said first spacers, and said second spacers.

25. (Original) The method in claim 24, further comprising, after removing said portion of said second spacers, doping portions of said first fin structure and said second fin structure that are not protected by said first spacers and said second spacers, such that there is a difference in doping between said first fin structure and said second fin structure.

26. (Original) The method in claim 25, wherein a difference in doping between said first fin structure and said second fin structure changes an effective width of said second fin structure when compared to said first fin structure.

27. (Original) The method in claim 22, wherein said first fin structure is the same size as said

second fin structure, wherein said width is a measure of distance in a direction perpendicular to the surface of said buried oxide layer.

28. (Original) The method in claim 22, wherein said first spacers and said second spacers comprise the same material.